Review of Soft Core Forth Processors

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Linked In Page

Uncensored Climate News

What is Forth?

Python

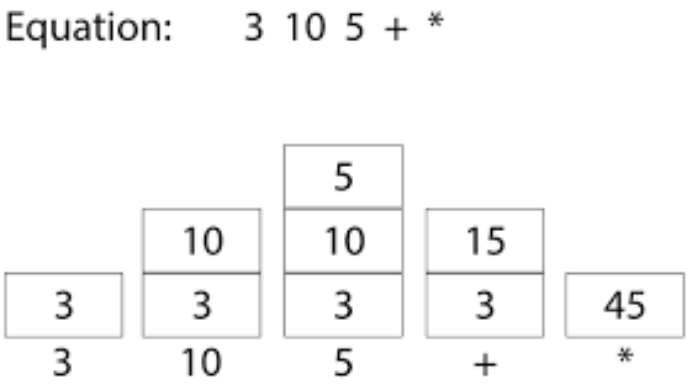
X= (10 + 5) * 3
print (x)

>>> 45

Forth

3 10 5 + * .

>>> 45



Historic Forth Processors

- RTX 2000
- Novix NC4016
- MISC MC17
- WISC CPU 16/32
- Lots more...

Parallax Propeller 2

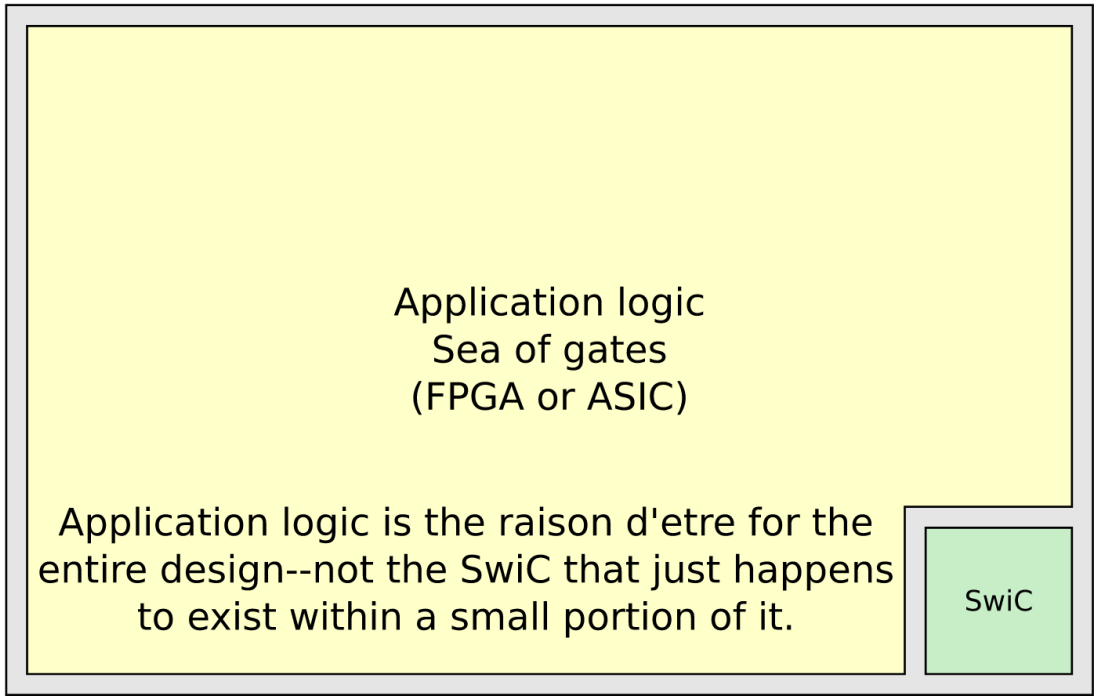
Parallax Propeller 2 has
8 cores 1024 * 32bits each
512 KB RAM every 8 cycles

Forth included in ROM

“TAQOZ Forth in ROM is implemented primarily for debugging hardware or testing out ‘what ifs’”.

-Peter Jackacki

System Within A Chip



"A SwiC is a small soft-core CPU within a chip, but specifically where the CPU is neither the purpose of the chip nor the main application within it." Dan Gisselquist Zip CPU.

Small Memory

Microblaze	J1
16380 Bytes	6349 Bytes

James Bowman found that the J1 required much less memory than the MicroBlaze soft core.

Small Device

ZPU	J1
442 Luts.	• 160 LUTS with a barrel shifter, 80 LUTS with 1 bit shifter.

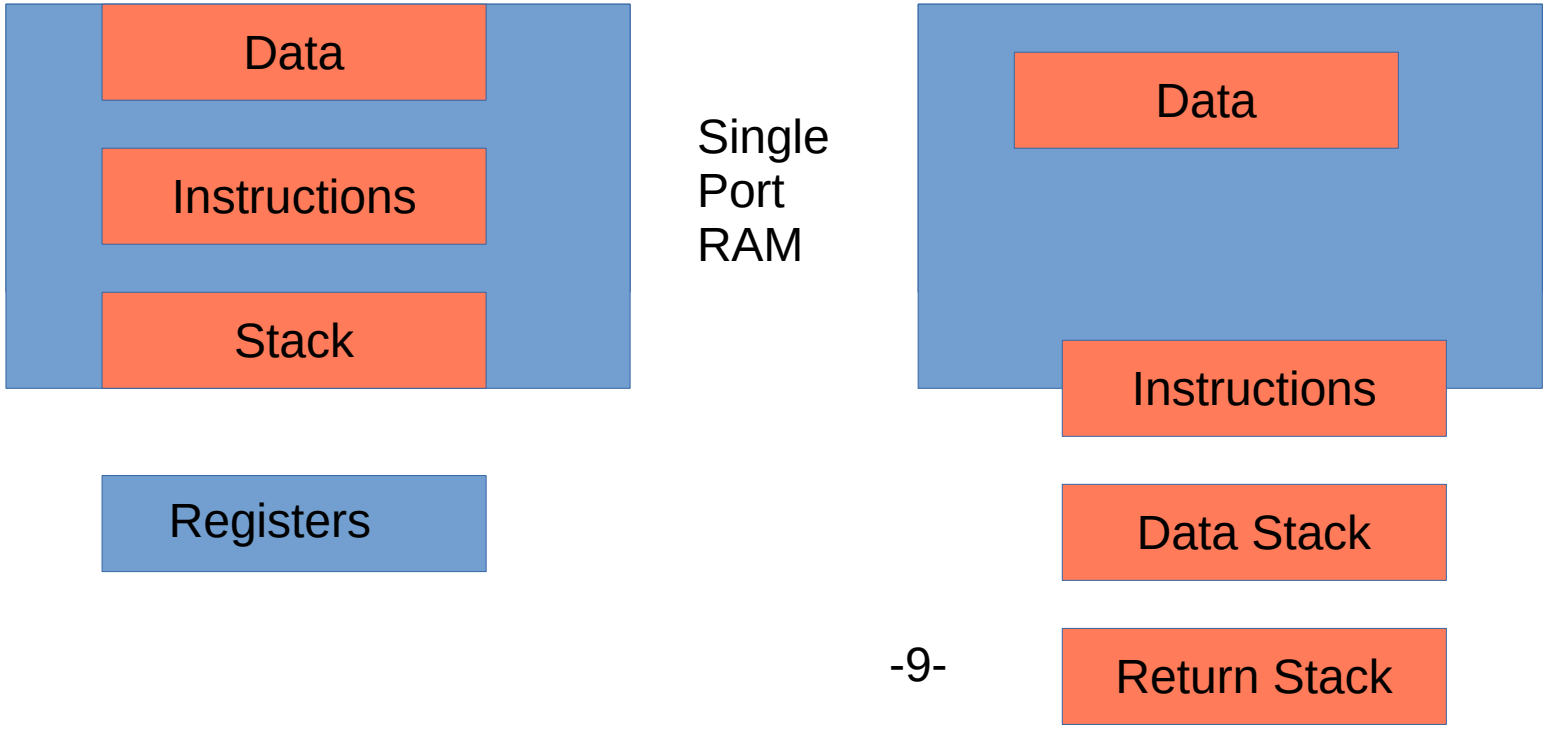
Why Forth/Stack Machines?

- Simple.
- Understandable.
- Modifiable.

Gnu C compiler has 16 million lines of code.

Less Memory Contention

- Register Machine (C) Stack Machine (Forth)



Constraints and Objectives

	Min Cost	RAM Limits	Min LUTs	Max Speed	Max Memory Efficiency	Max Application Speed	Port-ability	Min Work	Max Design Flexibility
J1	✓		✓	✓					
Mecrisp								✓	
Micro-Core		✓				✓			
EP16…					✓		✓		
J1Sc									✓
Core-1							✓	✓	
Hana-1	✓	✓			✓				
b16	✓				✓			✓	

Start With Dr. Ting's EP16/24/32/64

Beautifully Documented

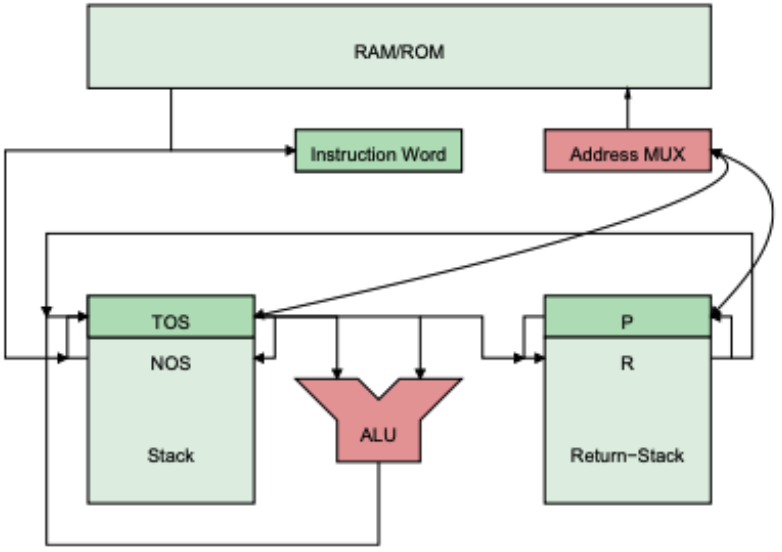
VHDL

Eforth has a big installed base on ESP32..

27 instructions

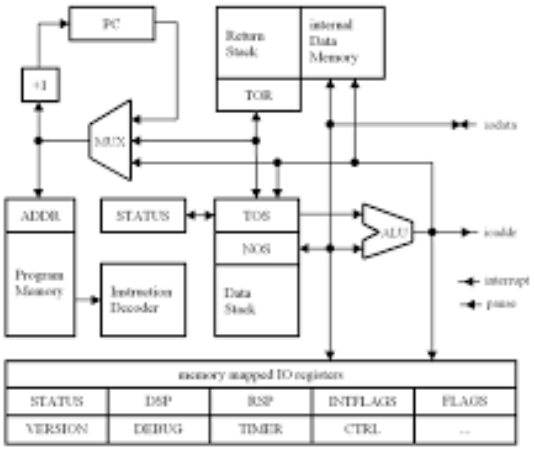
No traction

b16 Processor



Commercial Success.
Instructions are 5 bits each, and are packed 1-3 in each word.
Byte memory access is supported.
GPL

For complex applications: MicroCore



82 Instructions

Coroutines

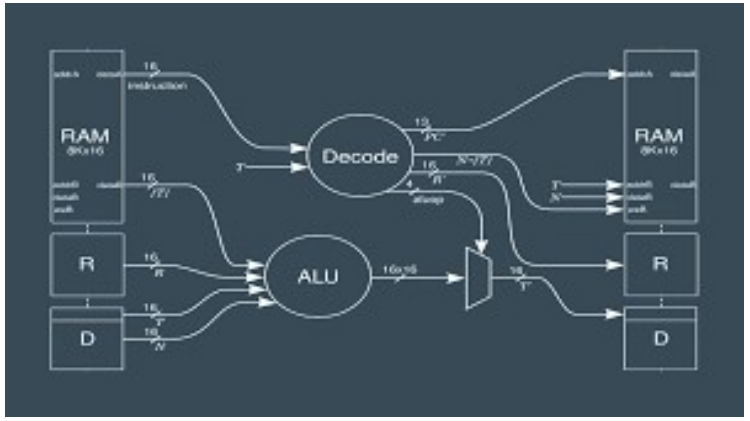
Variable Width Data

Variable Width Math

Runs everywhere

VHDL 83

For Speed and beauty: J1a,b



Small, Fast, Popular, and Brilliant.
But very limited.

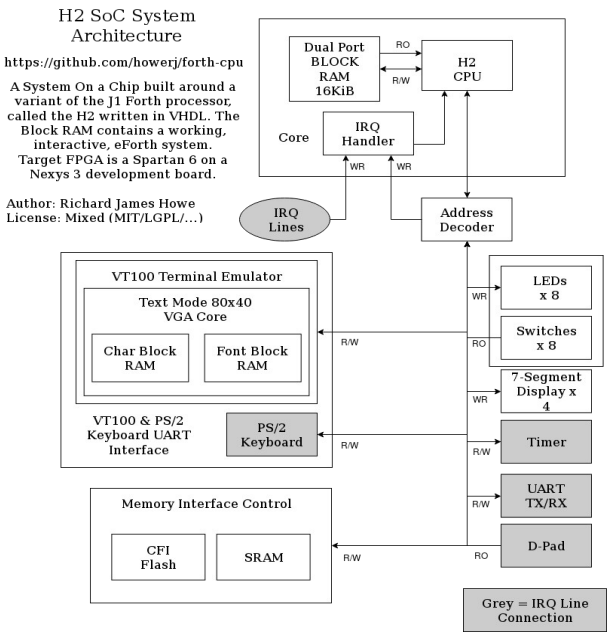
16 J1 Operations

0 T	8 N < T
1 N	9 N rshift T
2 T + N	10 T − 1
3 T and N	11 R
4 T or N	12 [T]
5 T xor N	13 N lshift T
6 ~ T	14 depth
7 N = T	15 N u<T

J1 Verilog Fragment

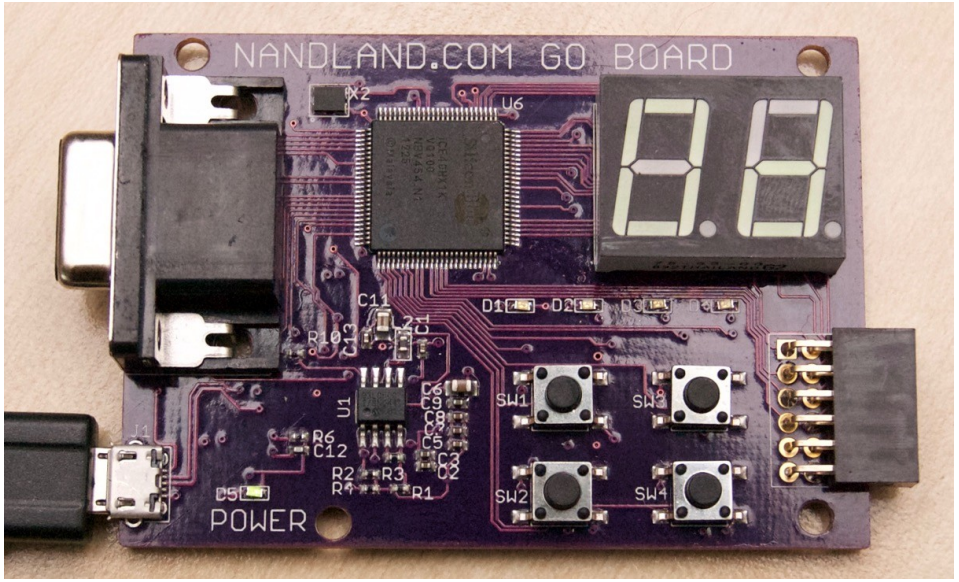
```
8'b000_?????: st0N = st0;                 // jump
8'b010_?????: st0N = st0;                 // call
8'b001_?????: st0N = st1;                 // conditional jump
8'b011_?0000: st0N = st0;                 // Duplicate Top of stack
8'b011_?0001: st0N = st1;                 // Duplicate Next of Stack
8'b011_?0010: st0N = st0 + st1;           //Add
8'b011_?0011: st0N = st0 & st1;           // And
8'b011_?0100: st0N = st0 | st1;           // Or
8'b011_?0101: st0N = st0 ^ st1;           //Xor
```

H2 Processor



- GPL Free Forth
- J1 Clone
- VHDL
- Interrupts
- C Simulator with VGA, Buttons, 7 bit display, and switches.
- Hold
- Stack Depth
- Cpu ID

Easy to use: Mecrisp-ICE



Enhanced version of Swapforth and the J1a

IO ports,

a tick counter,

constant folding,

inlining

tail-call optimisations.

SPI flash,

Run on boot. I

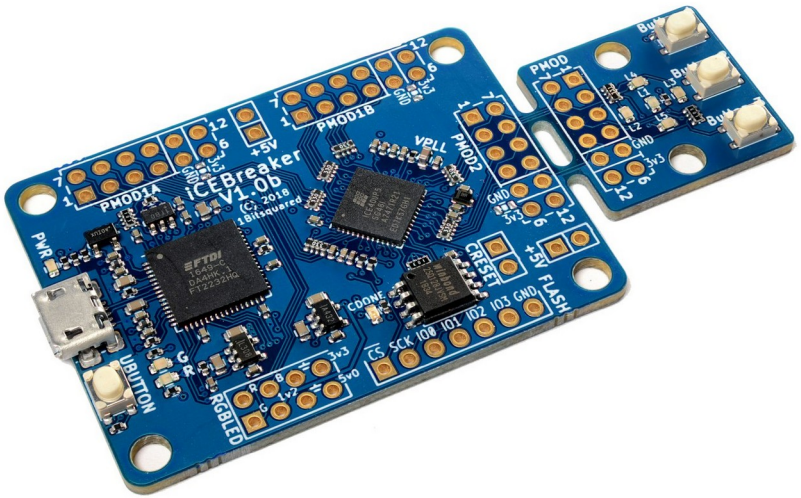
2 cycleInterrups

16 or 27 instructions

Mecrisp-Ice IceStick

Which board for you ?
If you just wish to play with a stack processor,
if you have small ideas,
if you desire to have IrDA communication,
if you wish a cheap, cool looking board,
if you are fine without tinkering with additional logic
  --> HX1K Icestick is your choice.

Recommended: Icebreaker



Lattice iCE40UP5k FPGA

5280 logic cells (4-LUT + Carry + FF)

120 Kbit dual-port block RAM

1 Mbit (128 KByte) single-port RAM

PLL, 2 x SPI, 2 x I2C hard IPs

Lots more...

MeCrisp-Ice HC8K

If you have large ideas in Forth,
if you need a lot of IO pins,
if you wish to wire in additional peripherals, opcodes or whatever you imagine,
if you love to have single cycle multiplier and barrel shifters

--> HX8K breakout board will give you a nice time.

Mecrisp Ice on the UPduino

Lattice UltraPlus ICE40UP5K FPGA with 5.3K LUTs, 1Mb SPRAM, 120Kb DPRAM, 8 Multipliers

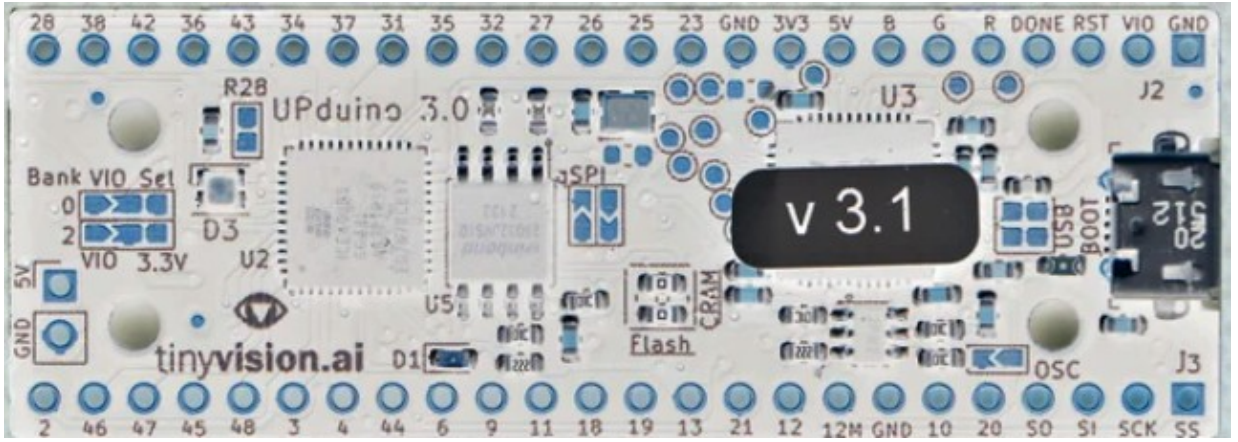
FTDI FT232H USB programmer with all pins brought out to test points

39 GPIO on 0.1” headers, 5V/3.3V/Ground to supply project DC power (<200mA)

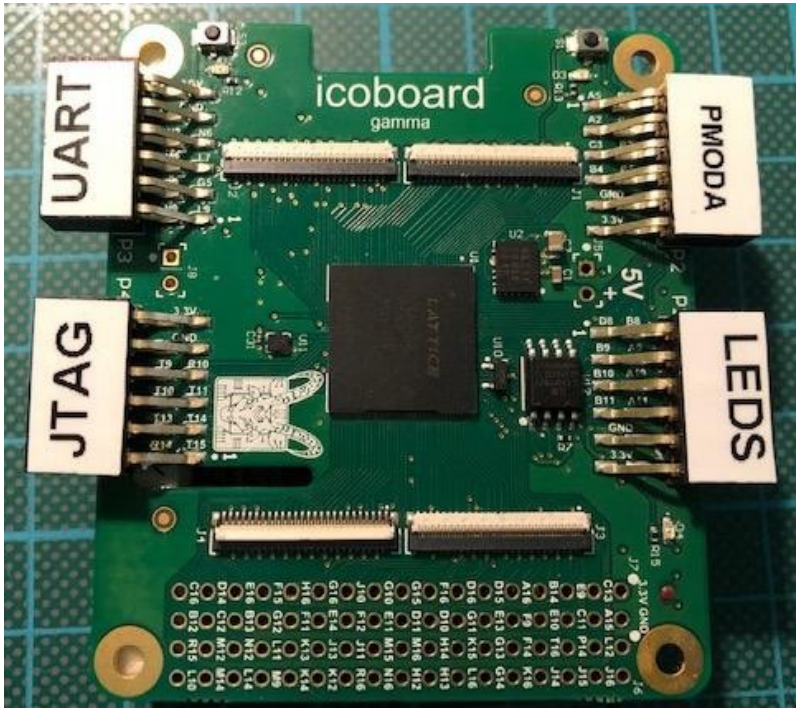
4MB qSPI SPI Flash

RGB LED

PMOD compatible



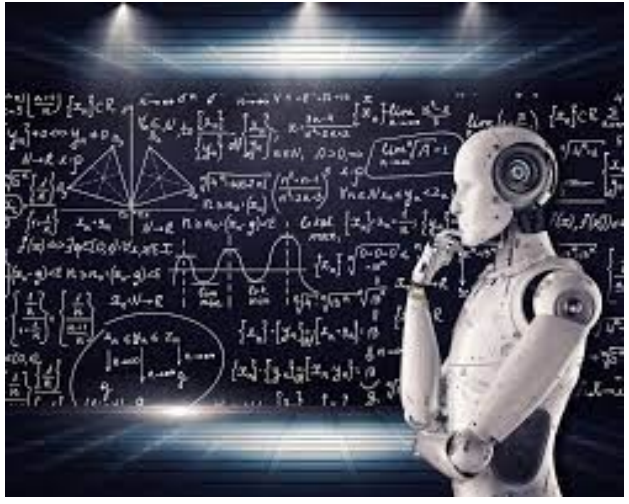
J1sc



A simple reimplementation of the J1 CPU in Scala using Spinal HDL.

The VexRiscV which won the first prize at the RISC-V Summit softCore contest, was also written in SpinalHDL.

Core-1



Written in System Verilog

Pause emphasized

72 Forth Words in Enum

No cross compiler needed

Code with AI

Embed in a larger FPGA project.

200 Facebook Members

Linked In Group

Simulators/Emulators

Verilator	SwapForth Mecrisp-Ice
C	H1 J1eForth
Python	SwapForth
Java	J1Sc
gForth	MicroCore

e4thcom

A Terminal for Embedded Forth Systems

Supported Forth Systems:

328eForth , 430CamelForth , 430eForth , 4e4th, AmForth, anyForth , Mecrisp , Mecrisp-Quintus , Mecrisp-Stellaris , noForth , STM8 eForth , SwapForth

Master’s Thesis

My approved Master’s thesis is to build a Forth CPU.

Now I understand the alternatives.

Hana 1

Port J1 to the iCE40UP5K FPGA on the Upduino using Single Port RAM.

Priority Memory.
Instruction Prefetch.

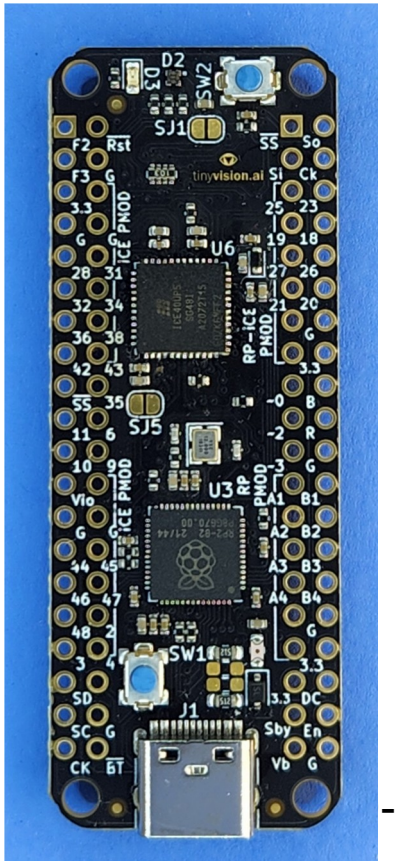
Instruction Compression?

Hana 3

Pico-Ice has an RP2040 and a iCE40UP5K FPGA.

RP2040
2 cores
256 KBytes RAM

ZeptoForth
Mecrisp Forth
No Forth



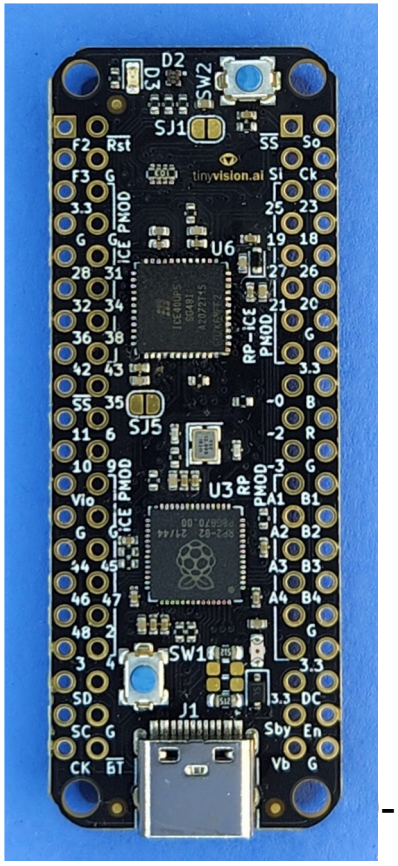
Ice40
1Mbit SPRAM
120 Kbits DPRAM

Mecrisp forth
SwapForth
eForth

Pico-Ice System Off a Chip $35

RP2040
2 cores
264 KBytes RAM

C,
MicroPython,
CircuitPython,
Go,
Rust,
JavaScript
Forth.

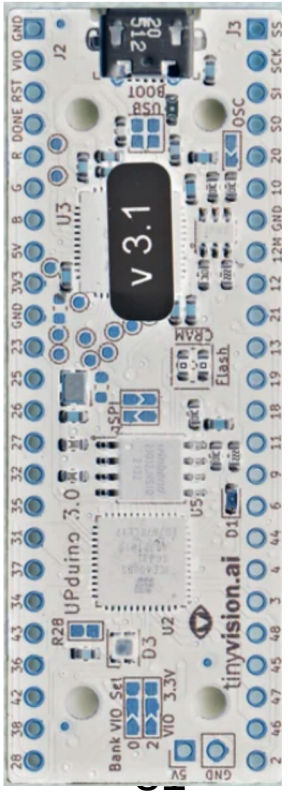


iCE40UP5K FPGA.
5280 LUTs
1Mbit SPRAM
120 Kbits DPRAM

Mecrisp Forth
SwapForth
eForth

Hana 8 on the UPduino

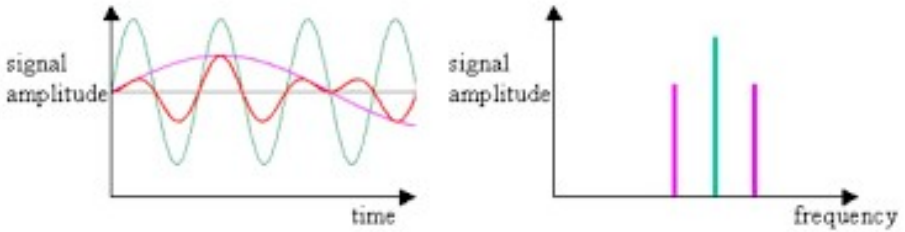
Propeller Parallax
$75
8 cores.
33Kbits each
1024 * 32 bit words
512 KBytes Shared
Ram every 8 cycles

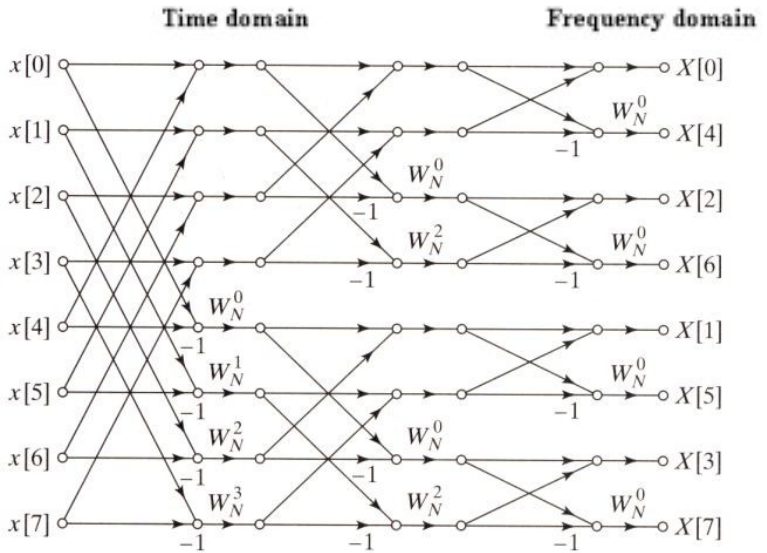


Hana 8 $30
4 Large Cores,
256Kbits each.
64K * 16 bit words.

4 Small Cores.
30Kbits each.
1875 *16 bit words.

Fourier Transform





Because it is under soft core control, not hard coded you can choose to do either:

16 bit FFT,

16 bit Floating point FFT,

32 bit FFT or

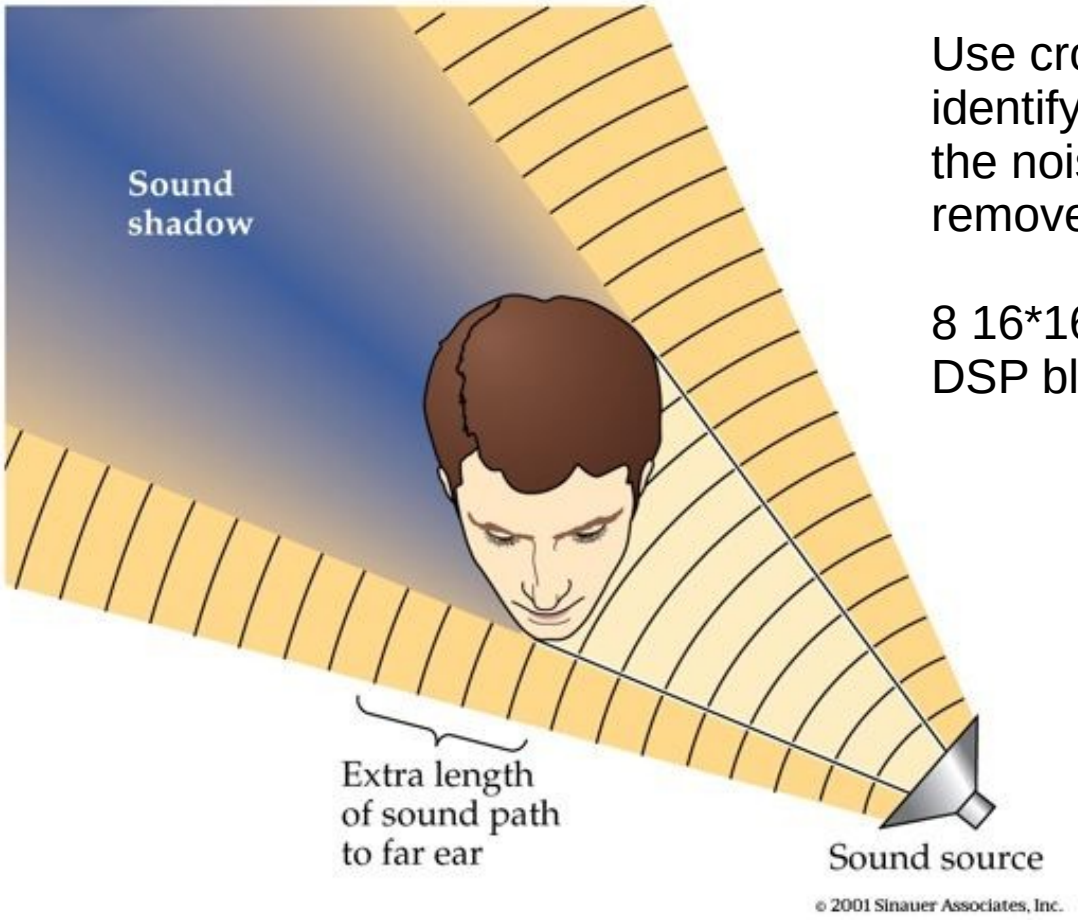
32 bit Floating Point FFT.

Hearing Aids

Computational Audiology is considering adding an FPGA device.

Stereo Audio is 16 bits.
Ice 40 is a low power FPGA with 8*16 bit multipliers.
Many older Forthers need it.

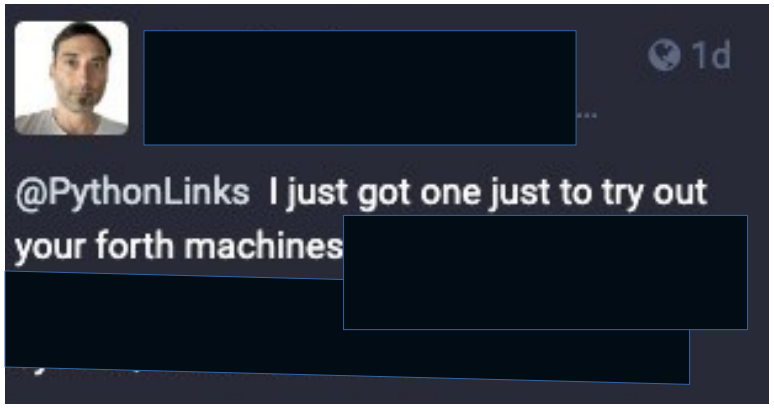
Sound localization

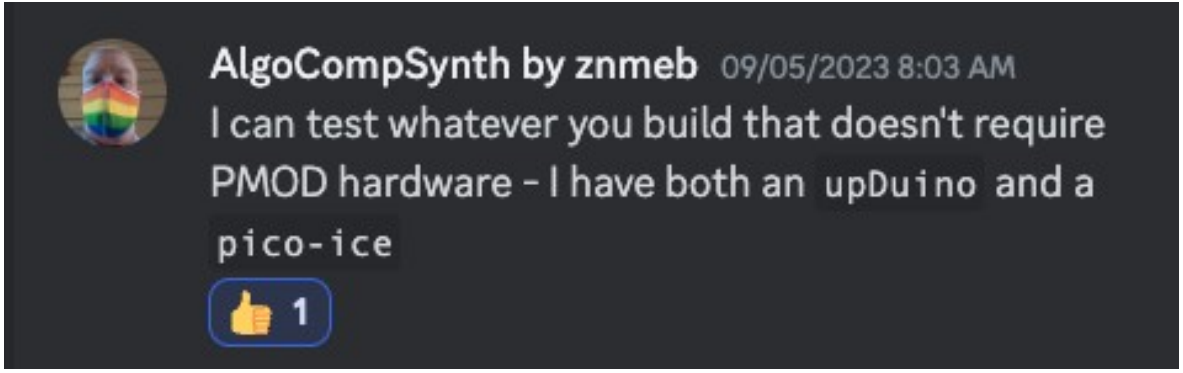


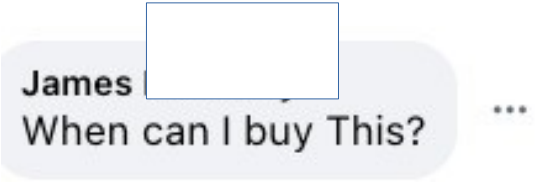
Use cross correlation to identify the angle of the noise sources and remove them.

8 16*16 multiply accumulate DSP blocks.

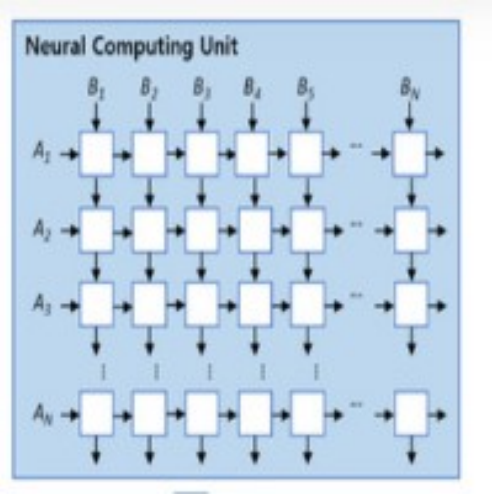
Reactions


1d
@PythonLinks I just got one just to try out
your forth machines


AlgoCompSynth by znmeb 09/05/2023 8:03 AM
I can test whatever you build that doesn't require
PMOD hardware - I have both an upDuino and a
pico-ice
1


James
When can I buy This?

Systolic Array For Vision



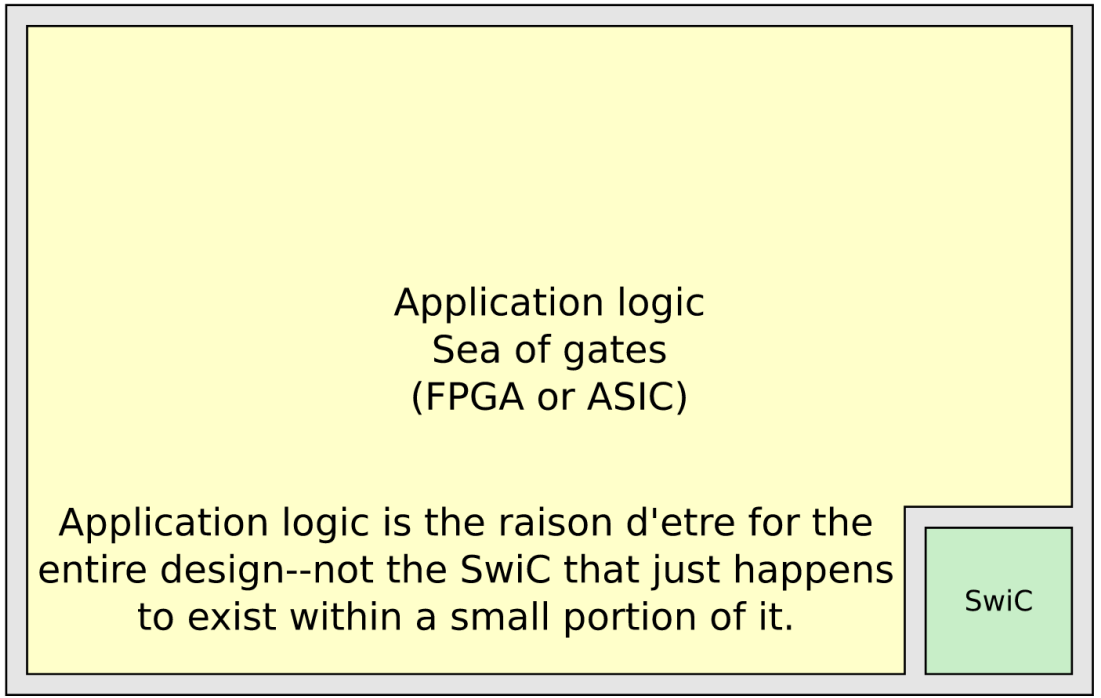
GreenArrays GA144 had
144 processors
but not enough memory

200px * 200px * 24 bits = 1Mbit

Constraints and Objectives

	Min Cost	RAM Limits	Min LUTs	Max Speed	Max Memory Efficiency	Max Application Speed	Port-ability	Min Work	Max Design Flexibility
J1	✓		✓	✓					
Mecrisp				✓				✓	
Micro-Core		✓				✓			
EP16					✓		✓		
J1Sc									✓
Core-1							✓	✓	✓
Hana-1	✓	✓			✓				
b16	✓				✓			✓	

System Within or Off a Chip



PacMan’s Blinky

“Every board should ship with a programable blinky demo using Forth.”

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Stockholm FPGA Conference
Sept 12, 2023

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